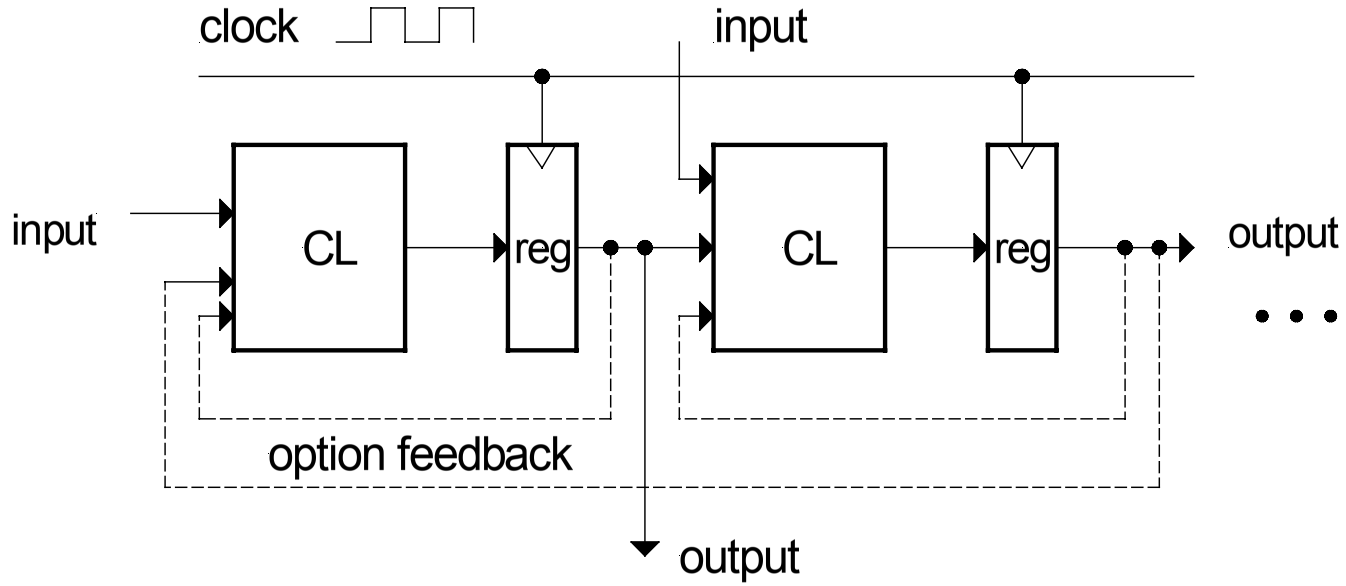
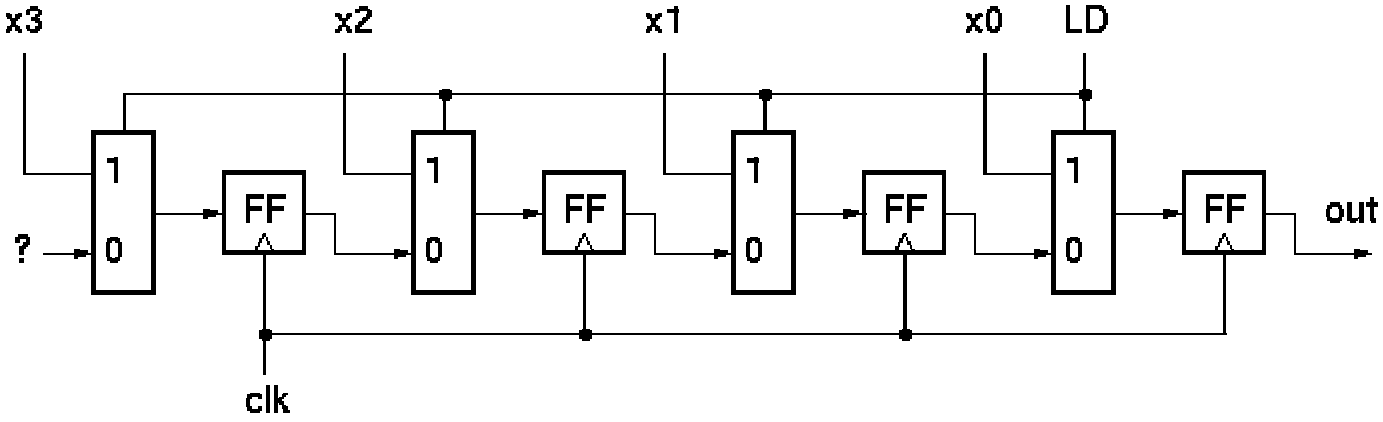
General Model of Synchronous Circuit



- All wires, except clock, may be multiple bits wide.
- Registers (reg)
  - collections of flip-flops
- clock
  - distributed to all flip-flops
  - typical rate?
- Combinational Logic Blocks (CL)
  - no internal state
  - output only a function of inputs
- Particular inputs/outputs are optional
- Optional Feedback

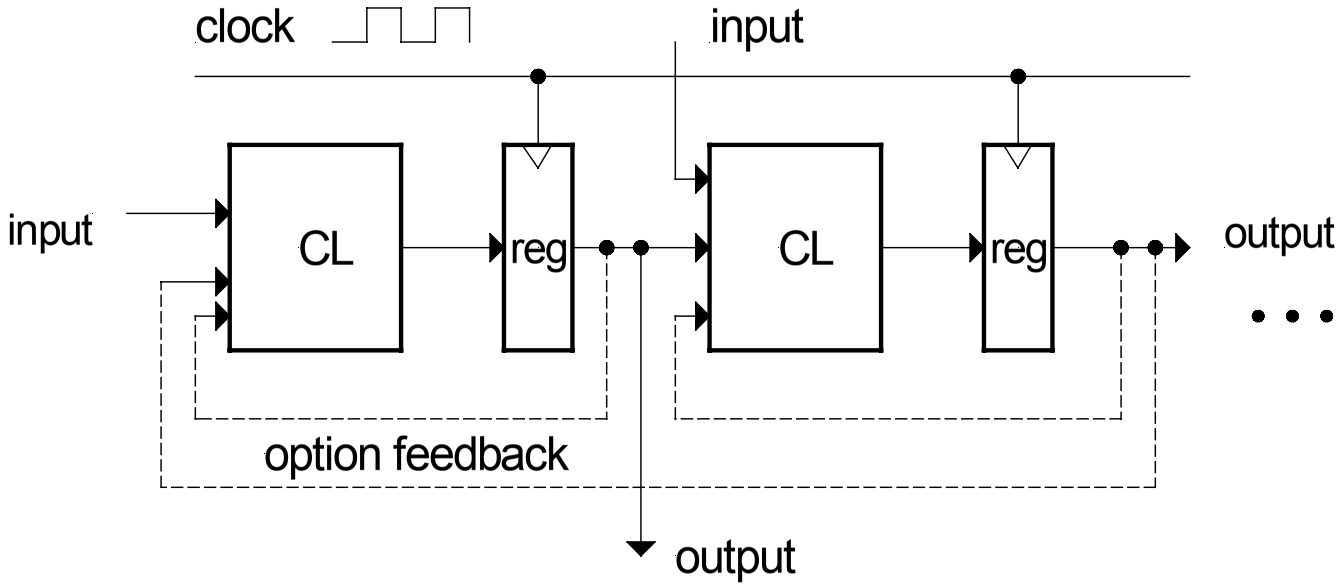
Example Circuit

- Parallel to Serial Converter



  - All signal paths single bit wide
  - Registers are single flip-flops
  - Combinational Logic blocks are simple multiplexors
  - No feedback in this case.

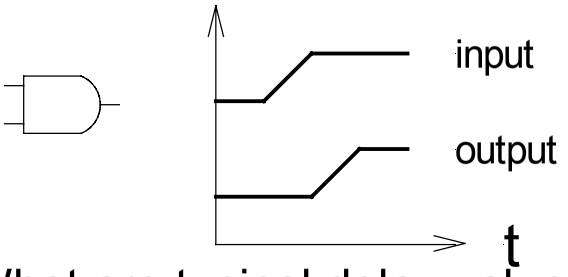
General Model of Synchronous Circuit



- How do we measure performance?
  - operations/sec?
  - cycles/sec?
- What limits the clock rate?
- What happens as we increase the clock rate?

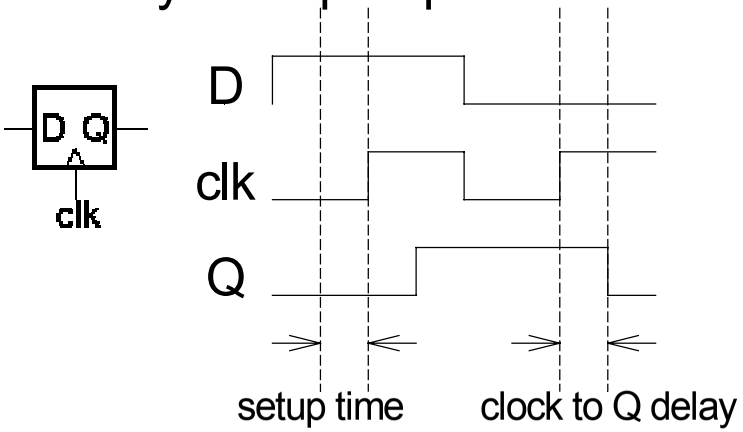
Limitations on Clock Rate

1 Logic Gate Delay



- What are typical delay values?

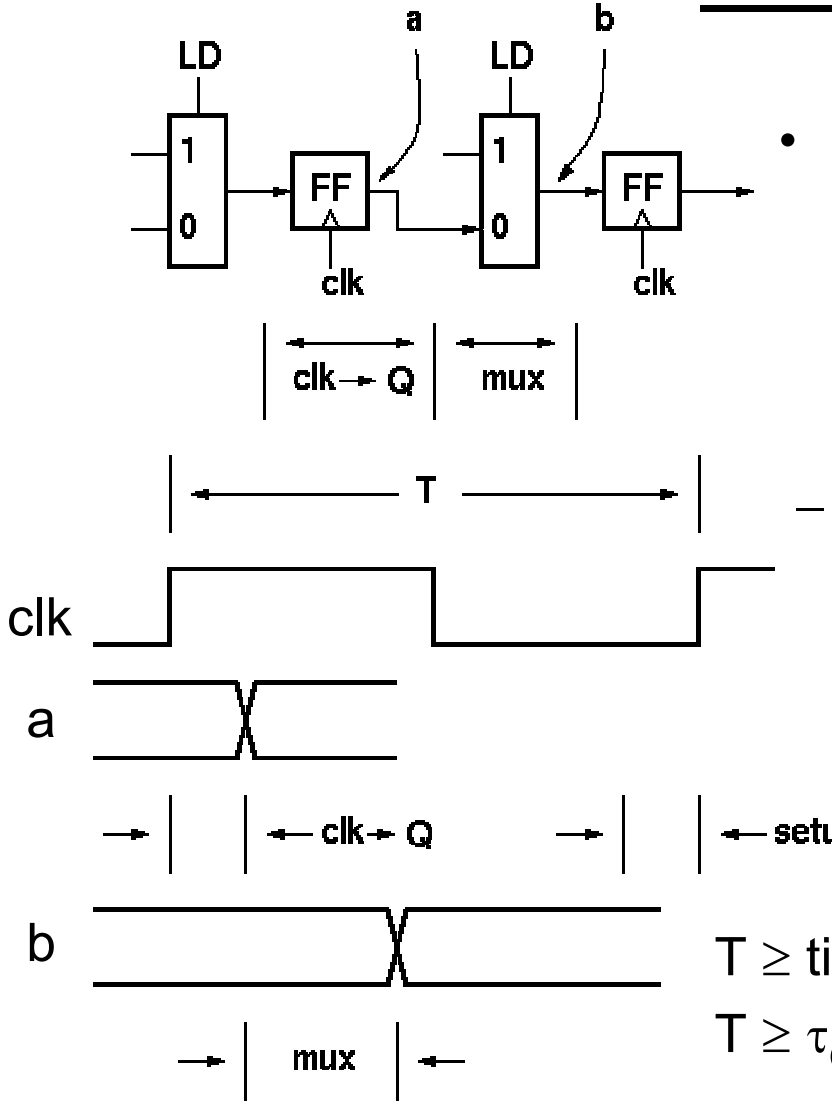
2 Delays in flip-flops



- Both times contribute to limiting the clock period.

- What must happen in one clock cycle for correct operation?
- Assuming perfect clock distribution (all flip-flops see the clock at the same time):
  - All signals must be ready and “setup” before rising edge of clock.

Example

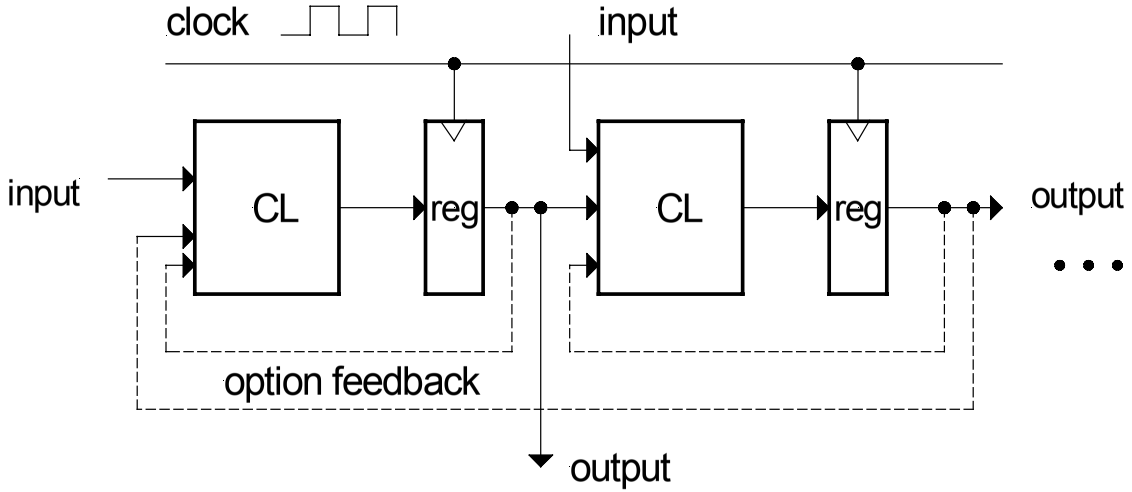


- Parallel to serial converter:

$T \geq \text{time}(\text{clk} \rightarrow Q) + \text{time}(\text{mux}) + \text{time}(\text{setup})$

$T \geq \tau_{\text{clk} \rightarrow Q} + \tau_{\text{mux}} + \tau_{\text{setup}}$

General Model of Synchronous Circuit



- In general, for correct operation:

$$T \geq \text{time}(\text{clk} \rightarrow Q) + \text{time}(CL) + \text{time}(\text{setup})$$

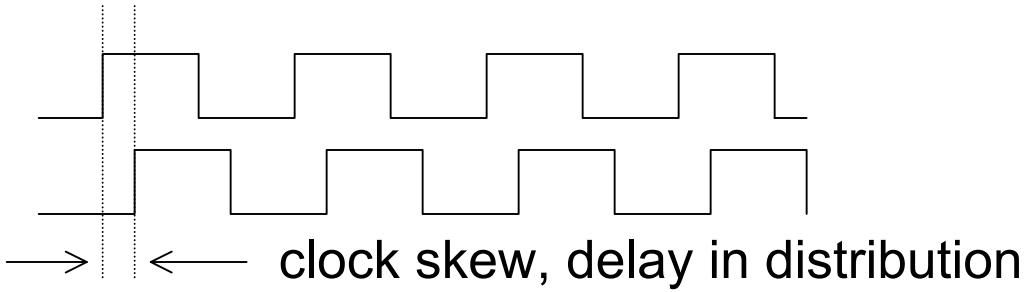
$$\boxed{T \geq \tau_{\text{clk}\rightarrow Q} + \tau_{CL} + \tau_{\text{setup}}}$$

for all paths.

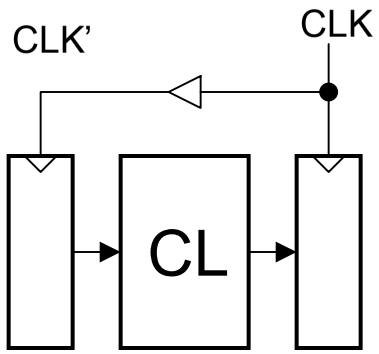
- How do we enumerate *all paths*?
  - Any circuit input or register output to any register input or circuit output.
  - "setup time" for circuit outputs depends on what it connects to
  - "clk-Q time" for circuit inputs depends on from where it comes.

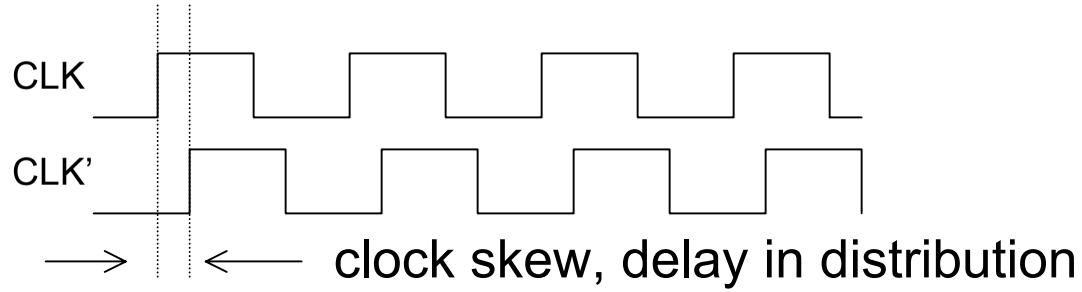
Clock Skew

- Unequal delay in distribution of the clock signal to various parts of a circuit:
  - if not accounted for, can lead to erroneous behavior.
  - Comes about because:
    - clock wires have delay,
    - circuit is designed with a different number of clock buffers from the clock source to the various clock loads, or
    - buffers have unequal delay.
  - All synchronous circuits experience some clock skew:
    - more of an issue for high-performance pipelined designs operating with very little extra time per clock cycle.



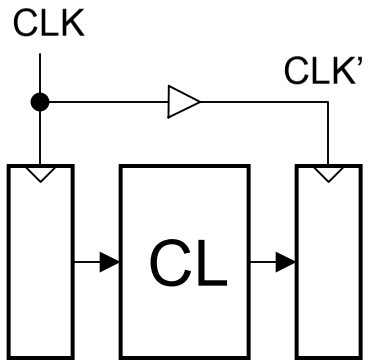
Clock Skew (cont.)

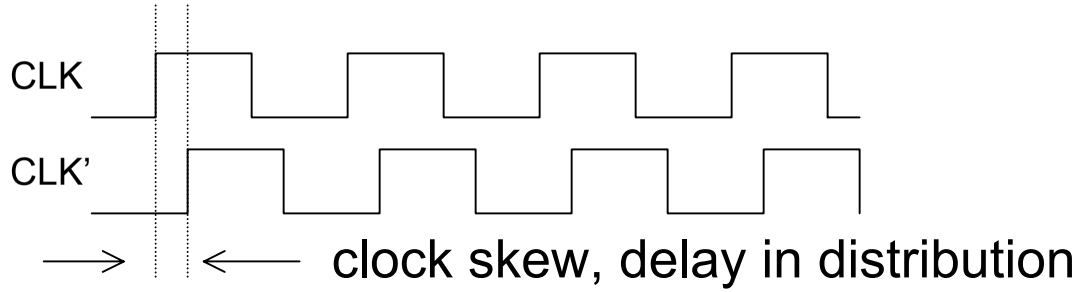




- If clock period $T = T_{CL}+T_{setup}+T_{clk\rightarrow Q}$, circuit will fail.
- Therefore:
  1. Control clock skew
     a) Careful clock distribution. Equalize path delay from clock source to all clock loads by controlling wires delay and buffer delay.
     b) don't "gate" clocks.
  2. $T \geq T_{CL}+T_{setup}+T_{clk\rightarrow Q}$ + worst case skew.
- Most modern large high-performance chips (microprocessors) control end to end clock skew to a few tenths of a nanosecond.

Clock Skew (cont.)





- Note reversed buffer.
- In this case, clock skew actually provides *extra time* (adds to the effective clock period).
- This effect has been used to help run circuits as higher clock rates. Risky business!